DK_VIDEO_GW5AT-LV60UG225_V1.0

User Guide

DBUG1281-1.0E, 03/07/2025

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Revision History

Date	Version	Description
03/07/2025	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The DK_VIDEO_GW5AT-LV60UG225_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the functions, circuits, and pin distributions of each hardware circuit.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- UG1222, GW5AT-60 Pinout
- UG983, GW5AT series of FPGA Products Package and Pinout User Guide
- UG718, Arora V 60K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDR	Double Data Rate
DP	Display Port

Terminology and Abbreviations	Meaning
DSI	Display Serial Interface
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
HDMI	High Definition Multimedia Interface
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
UART	Universal Asynchronous Receiver/Transmitter

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

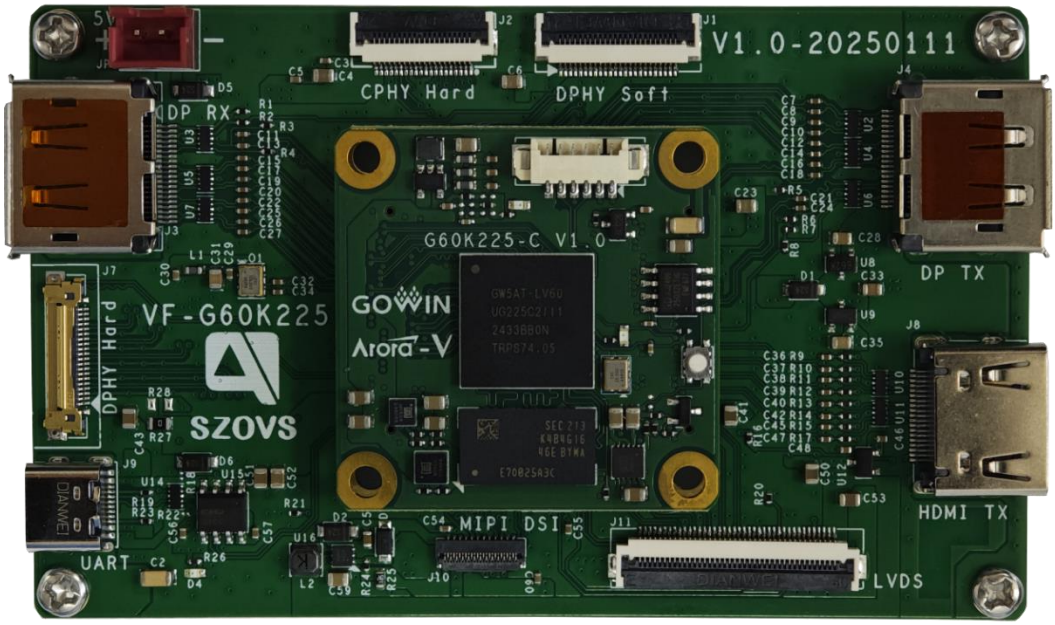
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_VIDEO_GW5AT-LV60UG225_V1.0 Development Board

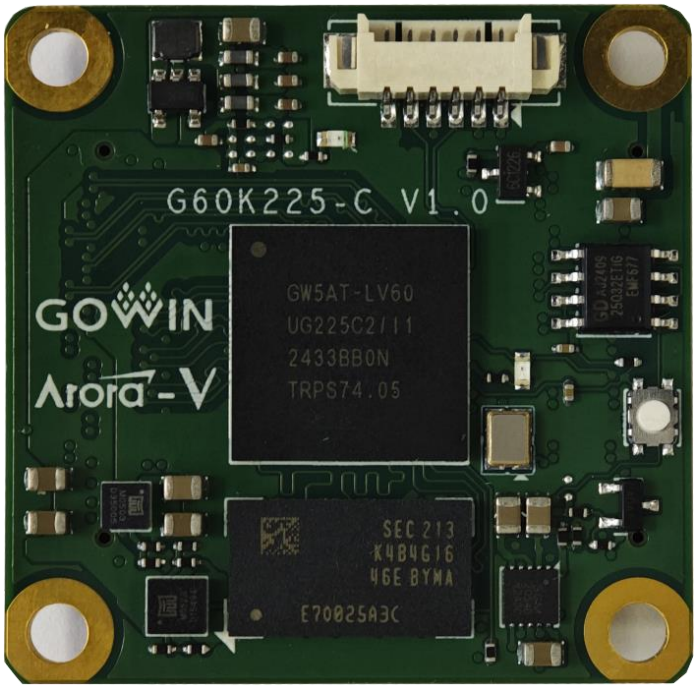


DK_VIDEO_GW5AT- LV60UG225_V1.0 development board applies to high-speed data storage based on DDR3, high-speed communication based on MIPI, SerDes, supporting MIPI C-PHY and MIPI D-PHY function evaluation, hardware verification, and software learning and debugging, etc.

The board consists of the DK_VIDEO_GW5AT-LV60UG225_V1.0 core board (hereinafter referred to as the core board) and the DK_VIDEO_GW5AT-LV60UG225_V1.0 carrier board (hereinafter referred to as the carrier board).

2.1.1 Core Board

Figure 2-2 DK_VIDEO_GW5AT-LV60UG225_V1.0 Core Board

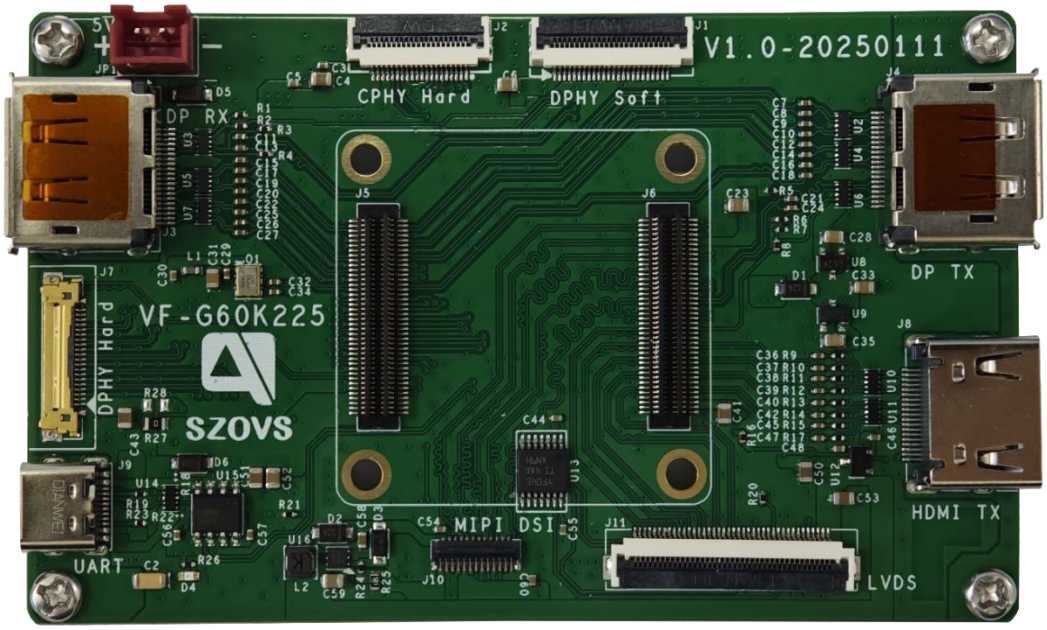


DK_VIDEO_GW5AT-LV60UG225_V1.0 core board adopts Gowin GW5AT series of FPGA devices, which is the 5 series products of Arora family with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3 and SerDes supporting multiple protocols and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design.

The core board adopts Gowin GW5AT-LV60UG225 FPGA device. For the internal resources of the chip, see *DS981, GW5AT series of FPGA Products Data Sheet*.

2.1.2 Carrier Board

Figure 2-3 DK_VIDEO_GW5AT-LV60UG225_V1.0 Carrier Board



The carrier board needs to be used with the DK_VIDEO_GW5AT-LV60UG225_V1.0 core board, integrated multiple interfaces, including LVDS, DP, HDMI, MIPI CPHY, MIPI DPHY, MIPI DPHY DSI, etc.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_VIDEO_GW5AT-LV60UG225_V1.0 core board
2. DK_VIDEO_GW5AT-LV60UG225_V1.0 carrier board
3. 1080*1920 MIPI LCD
4. 1024*600 LVDS/RGB LCD
5. SC130GS module with 1.3 MP MIPI global shutter black and white exposure
6. SC2210 module with 2 MP MIPI rolling shutter color exposure
7. IMX586 module with 48 MP CPHY rolling shutter color exposure
8. USB downloader
9. USB to Type-C cable

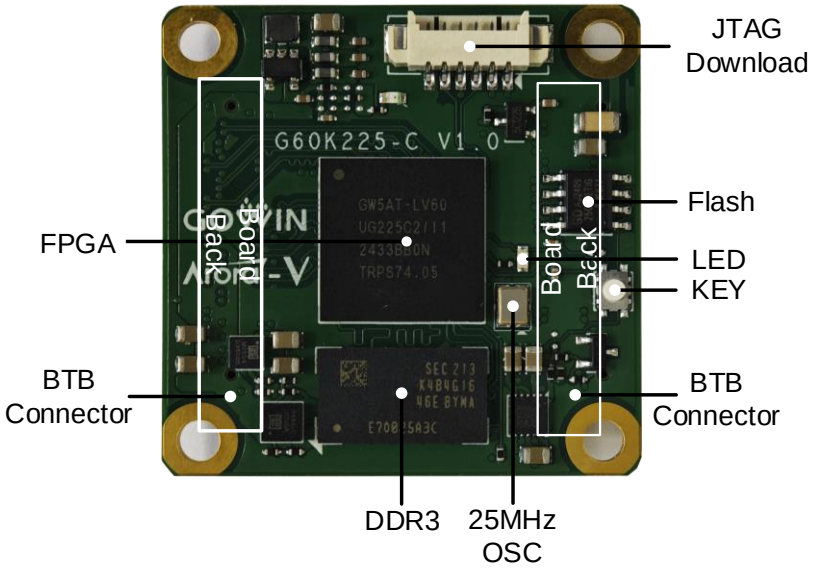
Figure 2-4 A Development Board Kit

① DK_VIDEO_GW5AT-LV60UG225_V1.0 core board
② DK_VIDEO_GW5AT-LV60UG225_V1.0 carrier board
③ 1080*1920 MIPI LCD
④ 1024*600 LVDS/RGB LCD
⑤ SC130GS module with 1.3 MP MIPI global shutter black and white exposure
⑥ SC2210 module with 2 MP MIPI rolling shutter color exposure
⑦ IMX586 module with 48 MP CPHY rolling shutter color exposure
⑧ USB downloader
⑨ USB to Type-C cable

2.3 PCB Components

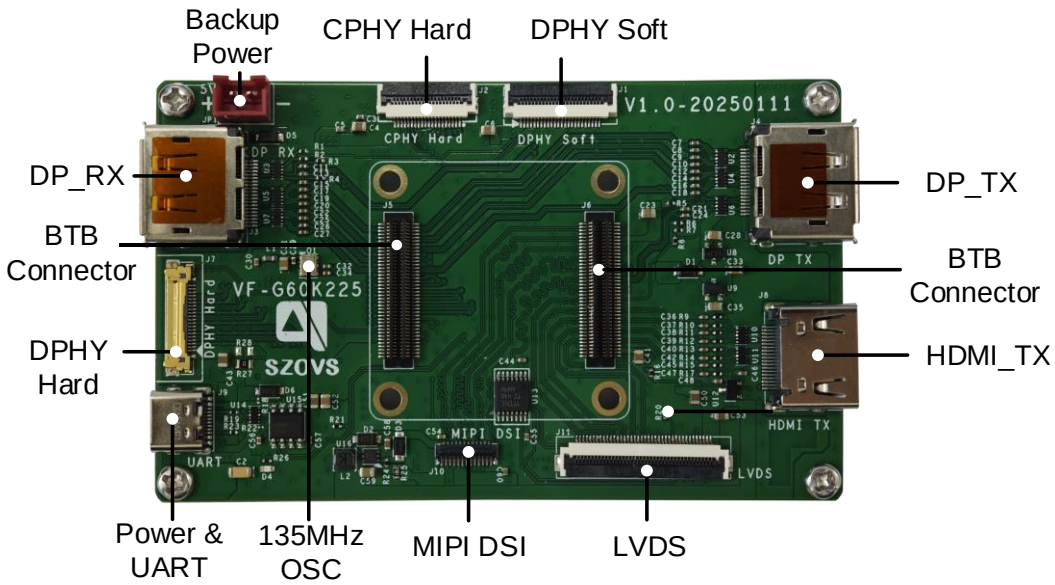
2.3.1 Core Board

Figure 2-5 PCB Components of Core Board



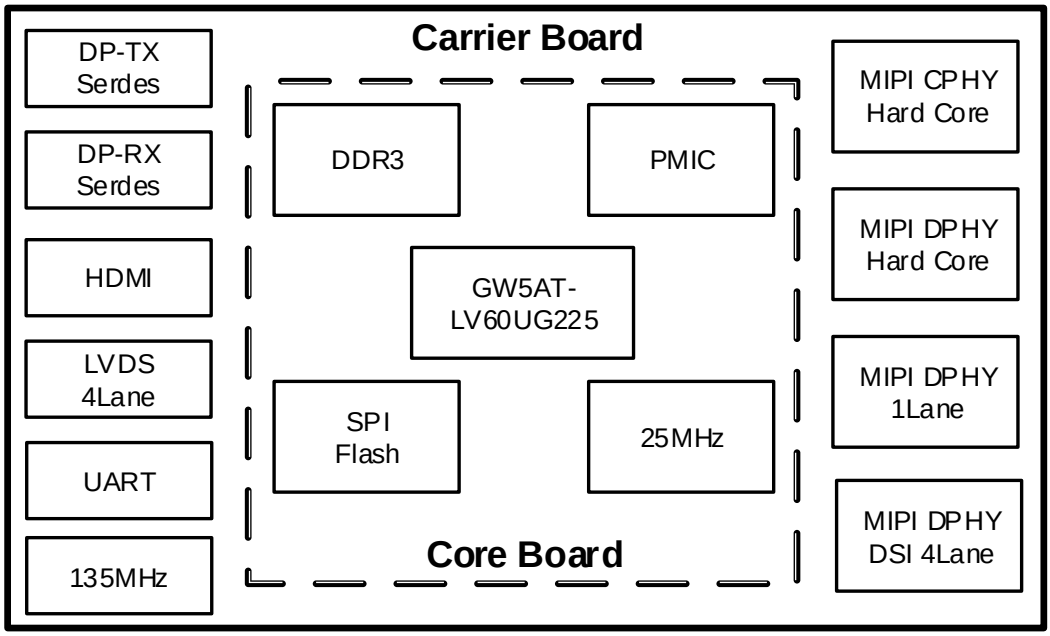
2.3.2 Carrier Board

Figure 2-6 PCB Components of Carrier Board



2.4 System Block Diagram

Figure 2-7 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AT-LV60UG225 FPGA
- Download and Boot
  - The core board integrates a JTAG interface and supports downloading via a USB downloader.
  - External Flash boot
  - The DONE light is on after loading
- Power
  - The 5V power supply is provided through the carrier board's USB to Type-C interface (J9) or XH2.54-2P pin header (JP1).
  - The carrier board powers the core board, which generates 3.3V, 1.8V, 1.5V, 1.2V, and 1.0V power supplies.
  - The carrier board generates 3.3V and 2.8V power supplies.
- Clock system
  - 1-channel 25 MHz single-ended clock
  - 1-channel 135 MHz differential clock
- Memory
  - 4Gbit DDR3 SDRAM
  - 32Mbit NOR Flash

- HDMI Interface
  - 1-channel HDMI interface
- DP Interface
  - 1-channel DP-TX interface
  - 1-channel DP-RX interface
  - Display Port connector
- MIPI Interface
  - 1-channel MIPI CPHY hard core, including 3*trios data
  - 1-channel MIPI DPHY hard core, including 4 data + 1 clk
  - 1-channel MIPI-DPHY soft core, including 4 data + 1 clk
  - 1-channel MIPI DPHY DSI, including 4 data+1 clk
- LVDS Interface
  - LVDS interface, including five pairs of differential signals (4 data+1 clk) and six control signals
- UART Interface
  - 1-channel UART interface
  - Use USB to Type-C connector
- Reset Key
  - One hard reset key, active-low
- Board-to-board Connector
  - Use two 80Pin board-to-board connector with 0.5mm pitch

3 Core Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW5AT series of FPGA products, refer to *DS981, GW5AT series of FPGA Products Data Sheet*.

3.1.2 I/O BANK Description

For the I/O BANK, package, and pinout information, see *UG983, GW5AT series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

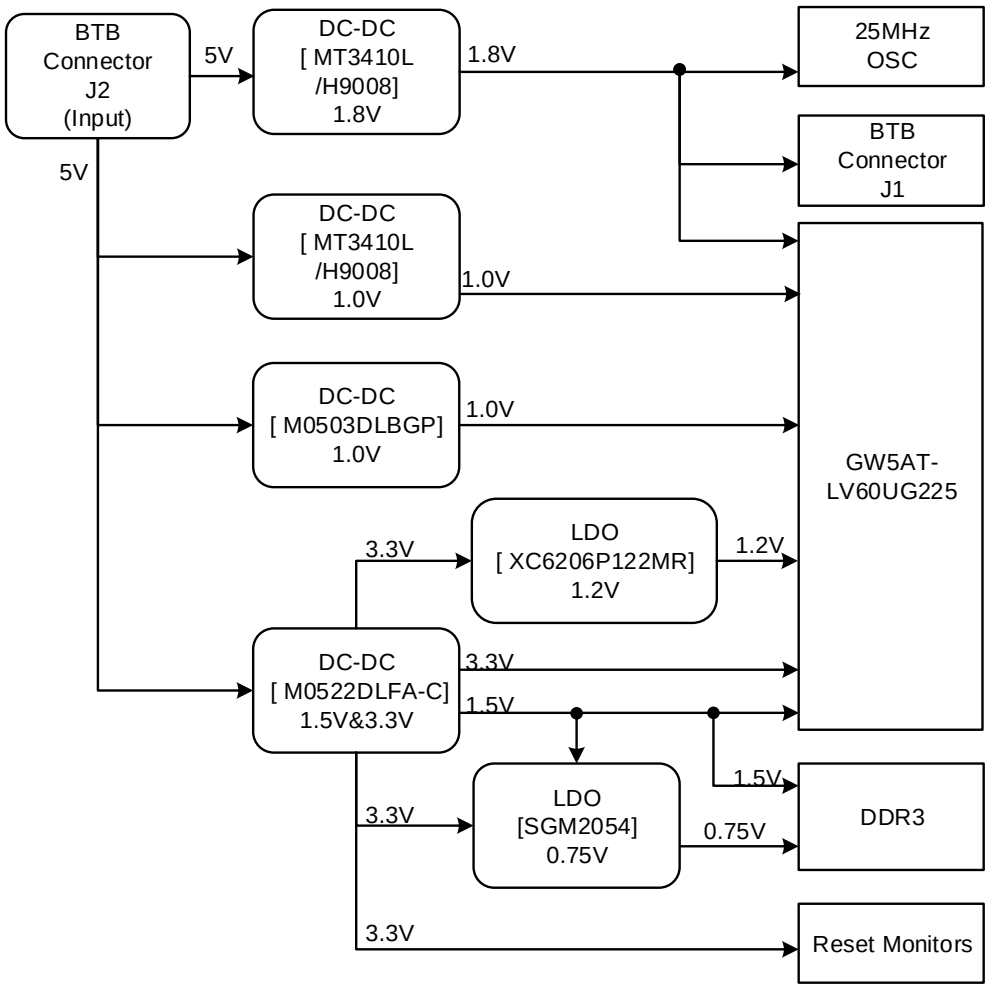
3.2.1 Introduction

The carrier board provides 5V power supply to the core board through the board-to-board connector.

The input 5V power supply is converted by the power management chip on the core board to generate 3.3V, 1.8V, 1.5V, 1.2V, and 1.0V power supplies to meet the power requirements of the core board.

3.2.2 Power System Distribution

Figure 3-1 Power Supply System Distribution



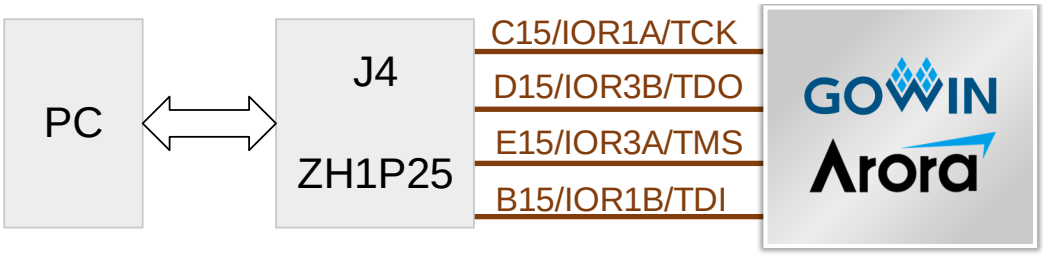
3.3 Download Module

3.3.1 Introduction

The development board includes a ZH1.25-6 pin header (J4) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is shown in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C15/IOR1A/TCK	C15	12	3.3V	JTAG signal
D15/IOR3B/TDO	D15	12	3.3V	
E15/IOR3A/TMS	E15	12	3.3V	
B15/IOR1B/TDI	B15	12	3.3V	

3.4 Clock

3.4.1 Introduction

The core board provides 1-channel 25 MHz single-ended clock.

Figure 3-3 Clock Connection Diagram

3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK25M	L6	9	1.5V	25 MHz single-ended clock

3.5 DDR3

3.5.1 Introduction

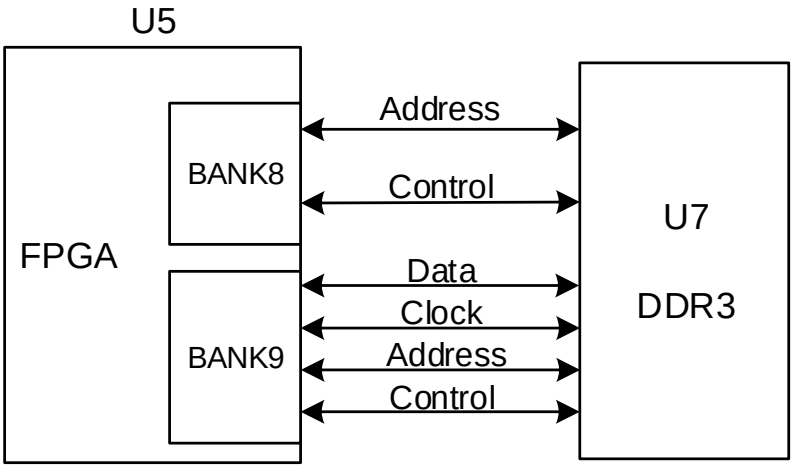
The development board includes one 4Gbit DDR3 chip. The signal of DDR3 chip is connected to the BANK8 and BANK9 of FPGA. The specific configurations of DDR3 are shown in Table 3-3.

Table 3-3 DDR3 Configuration

Designator	Capacity
U7	256M x 16bit

The hardware connection diagram of DDR3 is shown in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	R11	8	1.5V	Address
DDR3_A1	M9	9	1.5V	Address
DDR3_A2	N12	8	1.5V	Address
DDR3_A3	R10	8	1.5V	Address
DDR3_A4	N10	8	1.5V	Address
DDR3_A5	P11	8	1.5V	Address
DDR3_A6	L9	8	1.5V	Address
DDR3_A7	P13	8	1.5V	Address
DDR3_A8	M11	8	1.5V	Address
DDR3_A9	R12	8	1.5V	Address
DDR3_A10	L7	9	1.5V	Address
DDR3_A11	N11	8	1.5V	Address
DDR3_A12	N9	9	1.5V	Address
DDR3_A13	R13	8	1.5V	Address

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A14	M10	8	1.5V	Address
DDR3_BA0	N7	9	1.5V	Bank address
DDR3_BA1	L8	9	1.5V	Bank address
DDR3_BA2	P9	9	1.5V	Bank address
DDR3_CS#	R2	9	1.5V	Chip select
DDR3_CAS#	P2	9	1.5V	Column address strobe
DDR3_CKE	L10	8	1.5V	Clock Enable
DDR3_ODT	P1	9	1.5V	On-Die Termination Enable
DDR3_RAS#	N1	9	1.5V	Row address strobe
DDR3_RESET	R14	8	1.5V	Reset
DDR3_WE#	N2	9	1.5V	Write enable
DDR3_CLK0_P	N8	9	1.5V	Differential clock
DDR3_CLK0_N	M8	9	1.5V	Differential clock
DDR3_DQ0	L5	9	1.5V	Data
DDR3_DQ1	M6	9	1.5V	Data
DDR3_DQ2	M5	9	1.5V	Data
DDR3_DQ3	N6	9	1.5V	Data
DDR3_DQ4	P7	9	1.5V	Data
DDR3_DQ5	R7	9	1.5V	Data
DDR3_DQ6	R4	9	1.5V	Data
DDR3_DQ7	R5	9	1.5V	Data
DDR3_DQ8	M4	9	1.5V	Data
DDR3_DQ9	N5	9	1.5V	Data
DDR3_DQ10	M1	9	1.5V	Data
DDR3_DQ11	P5	9	1.5V	Data
DDR3_DQ12	L3	9	1.5V	Data
DDR3_DQ13	L1	9	1.5V	Data
DDR3_DQ14	N4	9	1.5V	Data

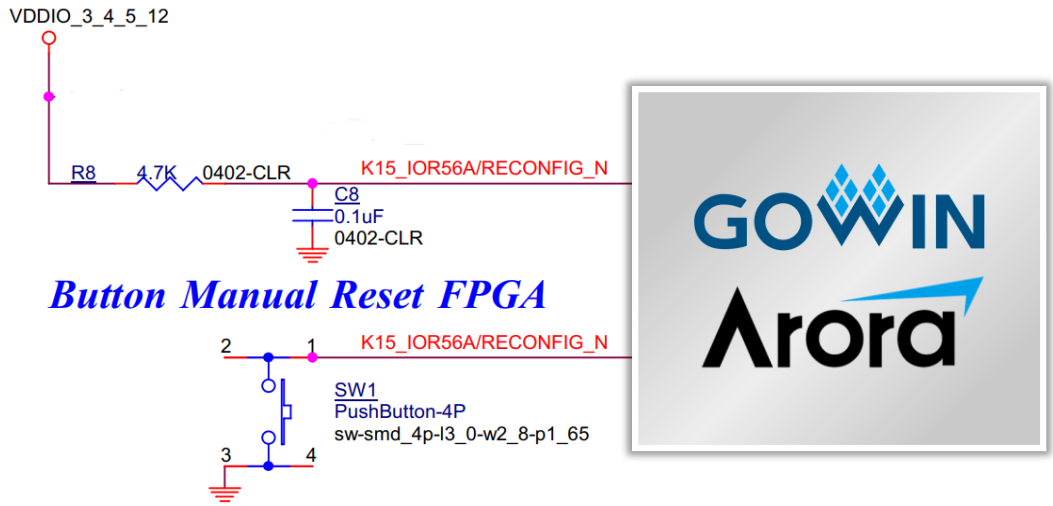
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ15	L2	9	1.5V	Data
DDR3_LDM0	R6	9	1.5V	Data input mask
DDR3_UDM0	M3	9	1.5V	Data input mask
DDR3_LDQS0_P	R8	9	1.5V	Data Clock
DDR3_LDQS0_N	R9	9	1.5V	Data Clock
DDR3_UDQS0_P	R3	9	1.5V	Data Clock
DDR3_UDQS0_N	P3	9	1.5V	Data Clock

3.6 Reset Key

3.6.1 Introduction

The core board includes one reset key, which is connected to the dedicated reset pin of FPGA BANK5. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-5.

Figure 3-5 Connection Diagram of Key



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K15_IOR56A/RECONFIG_N	K15	5	3.3V	Reset signal, active low

3.7 Board-to-board Connector

3.7.1 Introduction

The core board has two 80Pin board-to-board connector with 0.5mm pitch for communication with the DK_VIDEO_GW5AT-LV60UG225_V1.0 carrier board.

3.7.2 Pin Distribution

Table 3-6 Pin Distribution for J1 Board-to-Board Connector

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	GND	-	-	-	GND
3	D13_IOT146A/PLL/FB0/LVDS/DQ3	D13	2	1.2V	GPIO
4	B13_IOT142A/LVDS/DQ3	B13	2	1.2V	GPIO
5	C14_IOT146B/PLL/FB0/LVDS/DQ3	C14	2	1.2V	GPIO
6	A13_IOT142B/DOUT/LVDS/DQ3	A13	2	1.2V	GPIO
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	VDD3V3	-	-	3.3V	Power
10	B14_IOT144A/LVDS/DQ3	B14	2	1.2V	GPIO
11	VDD3V3	-	-	3.3V	Power
12	A14_IOT144B/LVDS/DQ3	A14	2	1.2V	GPIO
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	E10_IOT89B/GCLKC_1/LVDS/DQ0	E10	1	1.2V	GPIO
16	E6_IOT74B/LVDS/DQ0	E6	1	1.2V	GPIO
17	F10_IOT89A/GCLKT_1/LVDS/DQ0	F10	1	1.2V	GPIO
18	E5_IOT74A/LVDS/DQ0	E5	1	1.2V	GPIO

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
19	GND	-	-	-	GND
20	GND	-	-	-	GND
21	F13_IOR9B/CSI_B/MOSI/MI 0/LVDS	F13	3	3.3V	GPIO
22	E9_IOT78B/LVDS/DQ0	E9	1	1.2V	GPIO
23	F12_IOR9A/D00/DIN/MISO/ MI1/LVDS	F12	3	3.3V	GPIO
24	F8_IOT78A/LVDS/DQ0	F8	1	1.2V	GPIO
25	GND	-	-	-	GND
26	GND	-	-	-	GND
27	F11_IOR15A/D11/LVDS	F11	3	3.3V	GPIO
28	E14_IOR5B/MODE0/LVDS	E14	3	3.3V	GPIO
29	G11_IOR15B/D12/LVDS	G11	3	3.3V	GPIO
30	E13_IOR5A/CCLK/LVDS	E13	3	3.3V	GPIO
31	GND	-	-	-	GND
32	GND	-	-	-	GND
33	H12_IOR36B/GCLKC_5/PLL/ LVDS/DQ4	H12	4	3.3V	GPIO
34	E8_IOT76B/TPLL_C_IN0/LV DS/DQ0	E8	1	1.2V	GPIO
35	G12_IOR36A/GCLKT_5/PLL/ LVDS/DQ4	G12	4	3.3V	GPIO
36	E7_IOT76A/TPLL_T_IN0/LV DS/DQ0	E7	1	1.2V	GPIO
37	GND	-	-	-	GND
38	GND	-	-	-	GND
39	H10_IOR41B/D15/GCLKC_7 /LVDS	H10	5	3.3V	GPIO
40	G15_IOR17B/D10/GCLKC_4 /LVDS	G15	3	3.3V	GPIO
41	H11_IOR41A/D14/GCLKT_7/ LVDS	H11	5	3.3V	GPIO
42	F15_IOR17A/MODE1/GCLK	F15	3	3.3V	GPIO

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
	T_4/LVDS				
43	GND	-	-	-	GND
44	GND	-	-	-	GND
45	H13_IOR47A/DONE	H13	5	3.3V	GPIO
46	J14_IOR57B/GCLKC_6/LVDS/DQ5	J14	5	3.3V	GPIO
47	K15_IOR56A/RECONFIG_N	K15	5	3.3V	GPIO
48	J13_IOR57A/GCLKT_6/LVDS/DQ5	J13	5	3.3V	GPIO
49	GND	-	-	-	GND
50	GND	-	-	-	GND
51	G14_IOR20B/D02/MI3/LVDS/DQ4	G14	4	3.3V	GPIO
52	K11_IOR59B/LVDS/DQ5	K11	5	3.3V	GPIO
53	G13_IOR20A/D01/MI2/LVDS/DQ4	G13	4	3.3V	GPIO
54	J11_IOR59A/LVDS/DQ5	J11	5	3.3V	GPIO
55	GND	-	-	-	GND
56	GND	-	-	-	GND
57	J15_IOR34B/EMCCLK/LVDS/DQ4	J15	4	3.3V	GPIO
58	L14_IOR63B/D04/SSPI_CS_N/LVDS/DQS5	L14	5	3.3V	GPIO
59	H15_IOR34A/D13/LVDS/DQ4	H15	4	3.3V	GPIO
60	L13_IOR63A/D03/SI/SSI0/LVDS/DQS5	L13	5	3.3V	GPIO
61	GND	-	-	-	GND
62	GND	-	-	-	GND
63	K13_IOR61B/RDWR_B/SCL/PLL/LVDS/DQ5	K13	5	3.3V	GPIO
64	M13_IOR68B/LVDS/DQ5	M13	5	3.3V	GPIO
65	K12_IOR61A/D07/SDA/PLL/	K12	5	3.3V	GPIO

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
	LVDS/DQ5				
66	L12_IOR68A/LVDS/DQ5	L12	5	3.3V	GPIO
67	GND	-	-	-	GND
68	GND	-	-	-	GND
69	M15_IOR66B/D06/SSPI_CLK/PLL/LVDS/DQ5	M15	5	3.3V	GPIO
70	N15_IOR70B/D09/CLKHOLD_N/SSI3/LVDS/DQ5	N15	5	3.3V	GPIO
71	L15_IOR66A/D05/SO/SSI1/PLL/LVDS/DQ5	L15	5	3.3V	GPIO
72	N14_IOR70A/D08/SSPI_WPN/SSI2/LVDS/DQ5	N14	5	3.3V	GPIO
73	GND	-	-	-	GND
74	GND	-	-	-	GND
75	VDD1V8	-	-	1.8V	GND
76	P15_IOR72B/CSO_B/MCS_N/PLL/LVDS/DQ5	P15	5	3.3V	GPIO
77	VDD1V8	-	-	1.8V	Floating
78	P14_IOR72A/READY/RPLL1_T_IN0/LVDS/DQ5	P14	5	3.3V	GPIO
79	GND	-	-	-	GND
80	GND	-	-	-	GND

Table 3-7 Pin Distribution for J2 Board-to-Board Connector

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	GND	-	-	-	GND
3	Q0_TXP_3	D12	Q0	-	TX data signal of SerDes Q0
4	Q0_RXP_3	B11	Q0	-	RX data signal of SerDes Q0
5	Q0_TXN_3	C12	Q0	-	TX data signal of SerDes Q0
6	Q0_RXN_3	A11	Q0	-	RX data signal of SerDes Q0
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	Q0_TXP_2	D8	Q0	-	TX data signal of SerDes Q0
10	Q0_REFCLKP_1	D10	Q0	-	Reference clock of SerDes Q0
11	Q0_TXN_2	C8	Q0	-	TX data signal of SerDes Q0
12	Q0_REFCLKN_1	C10	Q0	-	Reference clock of SerDes Q0
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	Q0_TXP_1	D6	Q0	-	TX data signal of SerDes Q0
16	Q0_RXP_2	B9	Q0	-	RX data signal of SerDes Q0
17	Q0_TXN_1	C6	Q0	-	TX data signal of SerDes Q0
18	Q0_RXN_2	A9	Q0	-	RX data signal of SerDes Q0
19	GND	-	-	-	GND
20	GND	-	-	-	GND
21	Q0_REFCLKP_0	B5	Q0	-	Reference clock of

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
					SerDes Q0
22	Q0_RXP_1	B7	Q0	-	RX data signal of SerDes Q0
23	Q0_REFCLKN_0	A5	Q0	-	Reference clock of SerDes Q0
24	Q0_RXN_1	A7	Q0	-	RX data signal of SerDes Q0
25	GND	-	-	-	GND
26	GND	-	-	-	GND
27	Q0_TXN_0	C4	Q0	-	TX data signal of SerDes Q0
28	Q0_RXP_0	B3	Q0	-	RX data signal of SerDes Q0
29	Q0_TXP_0	D4	Q0	-	TX data signal of SerDes Q0
30	Q0_RXN_0	A3	Q0	-	RX data signal of SerDes Q0
31	GND	-	-	-	GND
32	GND	-	-	-	GND
33	CPHY0_D0A	D1	MIPI_M1	-	Data signal of MIPI CPHY
34	DPHY0_D3P	C1	MIPI_M0	-	Data signal of MIPI DPHY
35	CPHY0_D0B	E2	MIPI_M1	-	Data signal of MIPI CPHY
36	DPHY0_D3N	C2	MIPI_M0	-	Data signal of MIPI DPHY
37	CPHY0_D0C	E1	MIPI_M1	-	Data signal of MIPI CPHY
38	GND	-	-	-	GND
39	GND	-	-	-	GND
40	DPHY0_D2P	F4	MIPI_M0	-	Data signal of MIPI DPHY
41	CPHY0_D1A	F1	MIPI_M1	-	Data signal of

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
					MIPI CPHY
42	DPHY0_D2N	E3	MIPI_M0	-	Data signal of MIPI DPHY
43	CPHY0_D1B	G1	MIPI_M1	-	Data signal of MIPI CPHY
44	GND	-	-	-	GND
45	CPHY0_D1C	G2	MIPI_M1	-	Data signal of MIPI CPHY
46	DPHY0_CKP	G3	MIPI_M0	-	Data signal of MIPI DPHY
47	GND	-	-	-	GND
48	DPHY0_CKN	F3	MIPI_M0	-	Data signal of MIPI DPHY
49	CPHY0_D2A	H1	MIPI_M1	-	Data signal of MIPI CPHY
50	GND	-	-	-	GND
51	CPHY0_D2B	J1	MIPI_M1	-	Data signal of MIPI CPHY
52	DPHY0_D1P	H4	MIPI_M0	-	Data signal of MIPI DPHY
53	CPHY0_D2C	J2	MIPI_M1	-	Data signal of MIPI CPHY
54	DPHY0_D1N	H3	MIPI_M0	-	Data signal of MIPI DPHY
55	GND	-	-	-	GND
56	GND	-	-	-	GND
57	H5/IOL48A/GCLKT_17/LVDS	H5	10	1.8V	GPIO
58	DPHY0_D0P	J4	MIPI_M0	-	Data signal of MIPI DPHY
59	H6/IOL48B/GCLKC_17/LVDS	H6	10	1.8V	GPIO
60	DPHY0_D0N	J3	MIPI_M0	-	Data signal of MIPI DPHY

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
61	GND	-	-	-	GND
62	GND	-	-	-	GND
63	K5/IOL50A/GCLKT_16/LVDS	K5	10	1.8V	GPIO
64	F5/IOL41A/LVDS	F5	11	1.8V	GPIO
65	J5/IOL50B/GCLKC_16/LVDS	J5	10	1.8V	GPIO
66	G5/IOL41B/LVDS	G5	11	1.8V	GPIO
67	GND	-	-	-	GND
68	GND	-	-	-	GND
69	K4/IOL45A/GCLKT_18/LVDS	K4	11	1.8V	GPIO
70	GND	-	-	-	GND
71	K3/IOL45B/GCLKC_18/LVDS	K3	11	1.8V	GPIO
72	VDD5V	-	-	5.5V	Power
73	GND	-	-	-	GND
74	VDD5V	-	-	5.5V	Power
75	GND	-	-	-	GND
76	VDD5V	-	-	5.5V	Power
77	GND	-	-	-	GND
78	VDD5V	-	-	5.5V	Power
79	GND	-	-	-	GND
80	VDD5V	-	-	5.5V	Power

4 Backplane Circuit

4.1 Power Supply

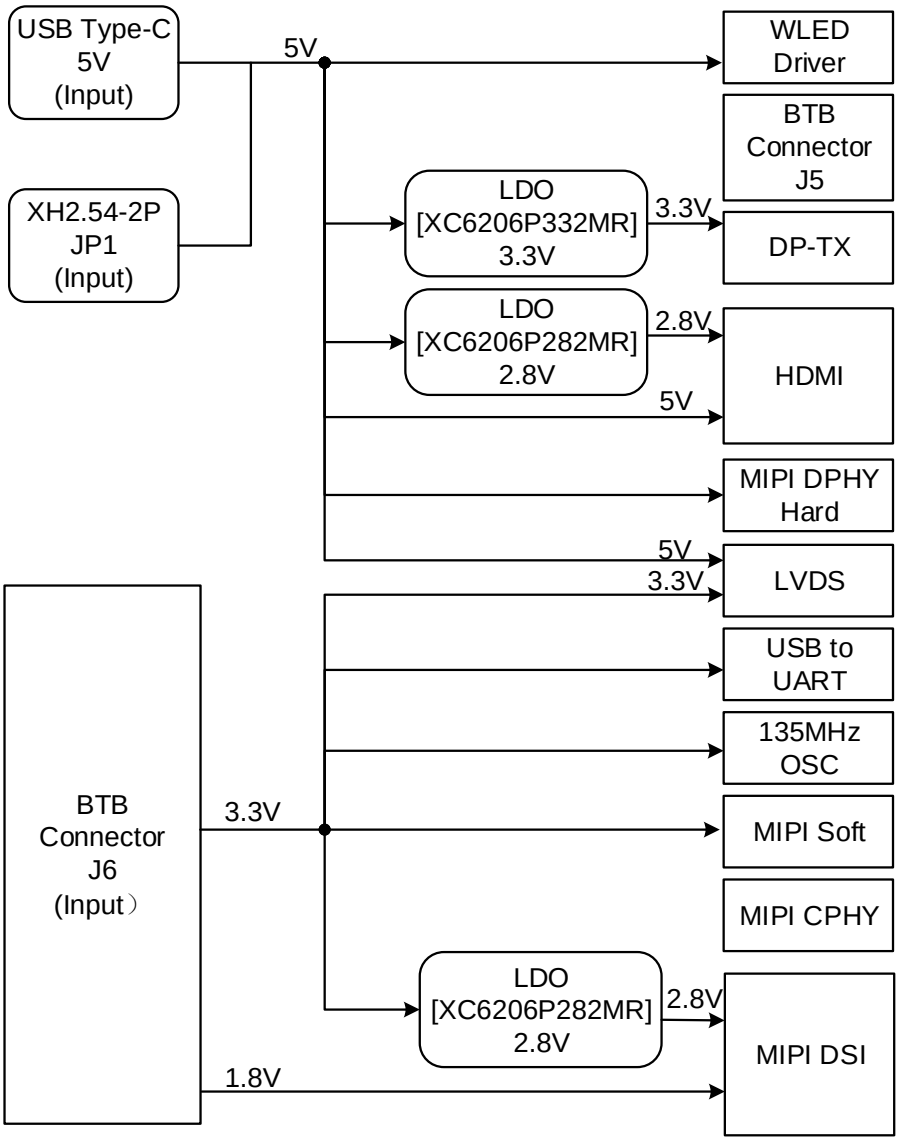
4.1.1 Introduction

The user can provide 5V power to the carrier board through the USB to Type-C interface (J9) or XH2.54-2P pin header (JP1). When using the XH2.54-2P pin header to provide 5V power supply, the 5V power from the USB to Type-C interface must be disconnected.

The input 5V power is converted by the power management chip on the carrier board to generate 3.3V and 2.8V power supplies. The core board provides 3.3V and 1.8V power supply to the carrier board through a board-to-board connector to meet the power requirements of the carrier board.

4.1.2 Power System Distribution

Figure 4-1 Power Supply System Distribution Diagram



4.2 Clock

4.2.1 Introduction

The carrier board includes 1-channel 135 MHz differential clock, connected to the FPGA SerDes high-speed clock pin via a board-to-board connector.

Figure 4-2 Clock Connection Diagram

4.2.2 Pin Distribution

Table 4-1 Clock Pin Distribution

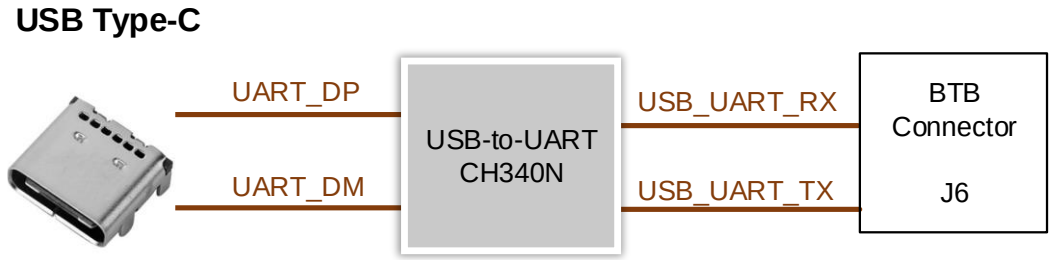
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
Q0_REFCLKP_0	B5	Q0	-	135 MHz differential clock
Q0_REFCLKN_0	A5	Q0	-	135 MHz differential clock

4.3 UART Interface

4.3.1 Introduction

The UART interface led from the development board uses USB to Type-C connector, which is implemented via USB conversion chips. The connection diagram of UART interface is shown in Figure 4-3.

Figure 4-3 Connection Diagram of UART Interface



4.3.2 Pin Distribution

Table 4-2 UART Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_UART_RX	H11	5	3.3V	Serial data output from FPGA
USB_UART_TX	H10	5	3.3V	Serial data input to FPGA

4.4 DP Interface

4.4.1 Introduction

The carrier board provides 1-channel DP-TX interface and 1-channel DP-RX interface. The connection diagram of the DP interfaces is as follows.

Figure 4-4 Connection Diagram of DP-TX Interface

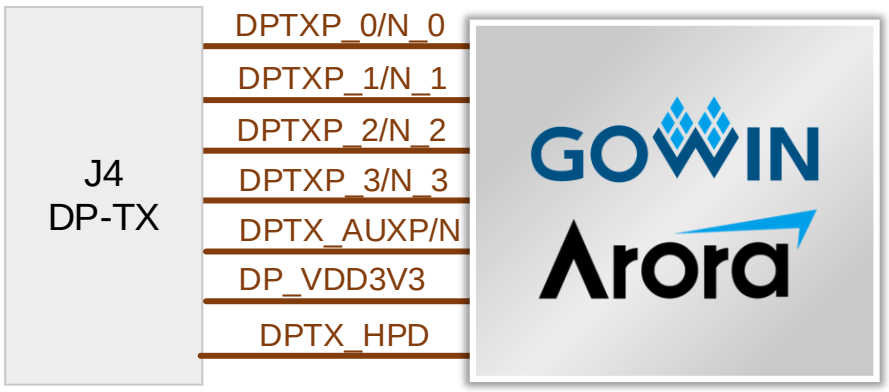
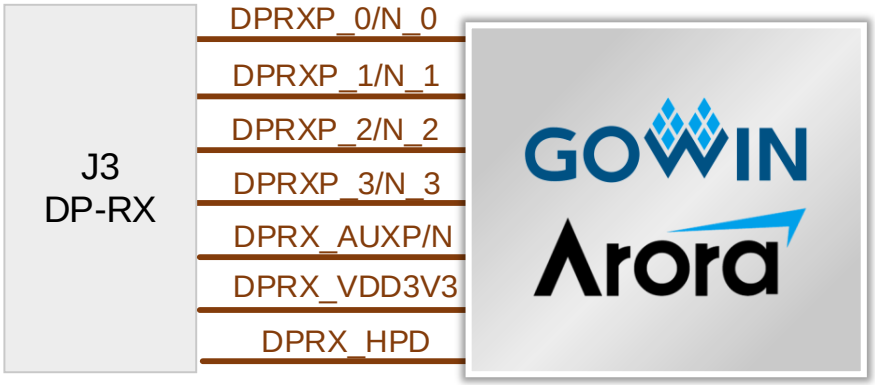


Figure 4-5 Connection Diagram of DP-RX Interface



4.4.2 Pin Distribution

Table 4-3 Pin Distribution of DP-TX Interface

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DPTXP_0	D12	Q0	-	DP Data Transmit
2	GND	-	-	-	GND
3	DPTXN_0	C12	Q0	-	DP Data Transmit

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
4	DPTXP_1	D8	Q0	-	DP Data Transmit
5	GND	-	-	-	GND
6	DPTXN_1	C8	Q0	-	DP Data Transmit
7	DPTXP_2	D6	Q0	-	DP Data Transmit
8	GND	-	-	-	GND
9	DPTXN_2	C6	Q0	-	DP Data Transmit
10	DPTXP_3	D4	Q0	-	DP Data Transmit
11	GND	-	-	-	GND
12	DPTXN_3	C4	Q0	-	DP Data Transmit
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	DPTX_AUXP	G12	4	3.3V	Auxiliary channel
16	GND	-	-	-	GND
17	DPTX_AUXN	H12	4	3.3V	Auxiliary channel
18	DPTX_HPD	H13	5	3.3V	Hot Plug Detect
19	GND	-	-	-	Floating
20	DP_VDD3V3	-	-	3.3V	Power

Table 4-4 Pin Distribution of DP-RX Interface

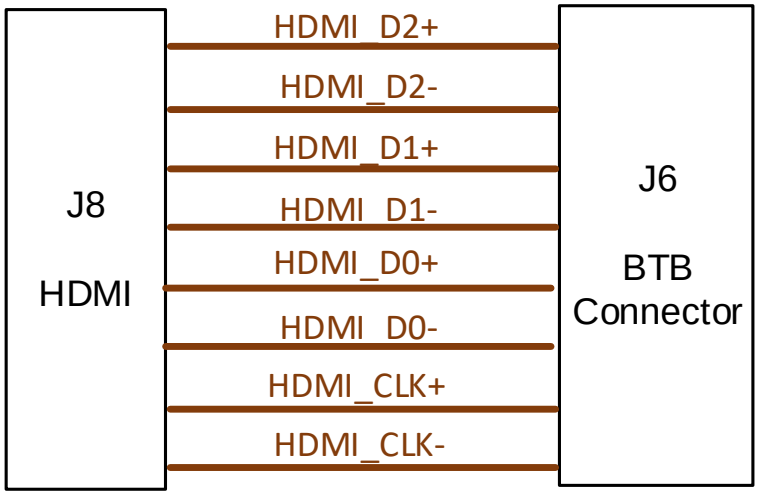
J3 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DPRXN_3	A3	Q0	-	DP Data Receive
2	GND	-	-	-	GND
3	DPRXP_3	B3	Q0	-	DP Data Receive
4	DPRXN_2	A7	Q0	-	DP Data Receive
5	GND	-	-	-	GND
6	DPRXP_2	B7	Q0	-	DP Data Receive
7	DPRXN_1	A9	Q0	-	DP Data Receive
8	GND	-	-	-	GND
9	DPRXP_1	B9	Q0	-	DP Data Receive
10	DPRXN_0	A11	Q0	-	DP Data Receive
11	GND	-	-	-	GND
12	DPRXP_0	B11	Q0	-	DP Data Receive
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	DPRX_AUXP	F11	3	3.3V	Auxiliary channel
16	GND	-	-	-	GND
17	DPRX_AUXN	G11	3	3.3V	Auxiliary channel
18	DPRX_HPD	E14	3	3.3V	Hot Plug Detect
19	NC	-	-	-	Floating
20	DPRX_VDD3V3	P14	5	3.3V	Power

4.5 HDMI Interface

4.5.1 Introduction

The development board provides an HDMI-TX interface for the transmitting of HDMI signals through an internal FPGA IP. The connection diagram of the interface is shown in Figure 3-5.

Figure 4-6 Connection Diagram of HDMI Interface



4.5.2 Pin Distribution

Table 4-5 HDMI Interface Pin Distribution

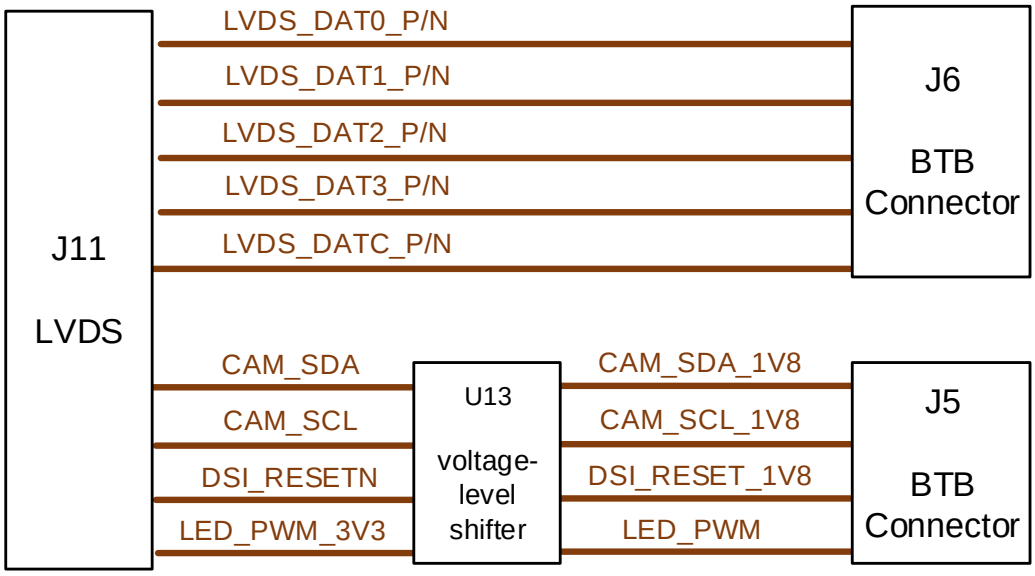
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI_CLK+	M15	5	3.3V	HDMI differential clock
HDMI_CLK-	L15	5	3.3V	HDMI differential clock
HDMI_D0+	K13	5	3.3V	HDMI transmit data
HDMI_D0-	K12	5	3.3V	HDMI transmit data
HDMI_D1+	J15	4	3.3V	HDMI transmit data
HDMI_D1-	H15	4	3.3V	HDMI transmit data
HDMI_D2+	G14	4	3.3V	HDMI transmit data
HDMI_D2-	G13	4	3.3V	HDMI transmit data

4.6 LVDS Interface

4.6.1 Introduction

The carrier board provides an LVDS display interface which uses a 40P FPC connector with 0.5mm pitch containing five pairs of differential signals and six control signals, respectively 4 data + 1 clk, I2C, reset, interrupt, PWM, and enable signals. The I2C, reset, and PWM signals are converted from four 1.8V logic signals from the FPGA on the core board to 3.3V logic signals through bidirectional level shifter chips on the carrier board, and then routed to the interface. The connection diagram is shown in Figure 4-7.

Figure 4-7 Connection Diagram of LVDS Interface



4.6.2 Pin Distribution

Table 4-6 LVDS Interface Pin Distribution

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	NC	-	-	-	Floating
2	NC	-	-	-	Floating
3	NC	-	-	-	Floating
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	GND	-	-	-	GND
7	GND	-	-	-	GND
8	LVDS_DAT0_N	J14	5	3.3V	LVDS signal
9	LVDS_DAT0_P	J13	5	3.3V	LVDS signal
10	GND	-	-	-	GND
11	LVDS_DAT1_N	K11	5	3.3V	LVDS signal
12	LVDS_DAT1_P	J11	5	3.3V	LVDS signal
13	GND	-	-	-	GND
14	LVDS_DAT2_N	L14	5	3.3V	LVDS signal
15	LVDS_DAT2_P	L13	5	3.3V	LVDS signal
16	GND	-	-	-	GND

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
17	LVDS_DATC_N	M13	5	3.3V	LVDS signal
18	LVDS_DATC_P	L12	5	3.3V	LVDS signal
19	GND	-	-	-	GND
20	LVDS_DAT3_N	N15	5	3.3V	LVDS signal
21	LVDS_DAT3_P	N14	5	3.3V	LVDS signal
22	GND	-	-	-	GND
23	NC	-	-	-	Floating
24	NC	-	-	-	Floating
25	GND	-	-	-	GND
26	CAM_SDA	H6	10	1.8V	Serial data signal of touchscreen
27	CAM_SCL	H5	10	1.8V	Serial clock signal of touchscreen
28	DSI_RESETN	K4	11	1.8V	Reset signal of touchscreen
29	CTP_INT	-	-	-	Interrupt signal of touchscreen
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	GND	-	-	-	GND
33	GND	-	-	-	GND
34	NC	-	-	-	Floating
35	LED_PWM_3V3	K3	11	1.8V	PWM signal of LED backlight
36	LCD_BLEN	-	-	-	Enable signal of LED backlight
37	NC	-	-	-	Floating
38	VDD5V	-	-	5V	Power
39	VDD5V	-	-	5V	Power
40	VDD5V	-	-	5V	Power

4.7 MIPI Interface

4.7.1 Introduction

The carrier board provides 1-channel MIPI DPHY hard core interface, 1-channel MIPI DPHY hard core interface, 1-channel MIPI DPHY soft core interface, and 1-channel MIPI DPHY DSI interface.

MIPI CPHY hard core (3*trios data), I2C, and reset signals are routed to 20P FPC connectors with 0.5mm pitch.

MIPI DPHY hard core signals (4 data + 1 clk) and two 1.8V standard GPIOs are routed to a 20P ultra-fine coaxial connector with 0.5mm pitch.

MIPI DPHY soft core (1 data + 1 clk) and I2C signals are routed to 24P FPC connectors with 0.5mm pitch.

The MIPI DPHY soft core (4 data + 1 clk) and reset signals of the MIPI DPHY DSI interface are routed to the 25P FPC connector with 0.3 mm pitch.

The connection diagrams of the interfaces are as follows.

Figure 4-8 Connection Diagram of MIPI CPHY Hard Core Interface

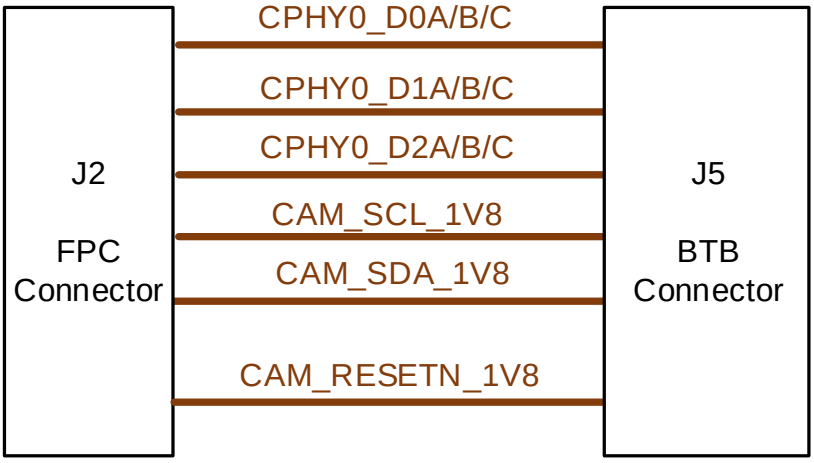
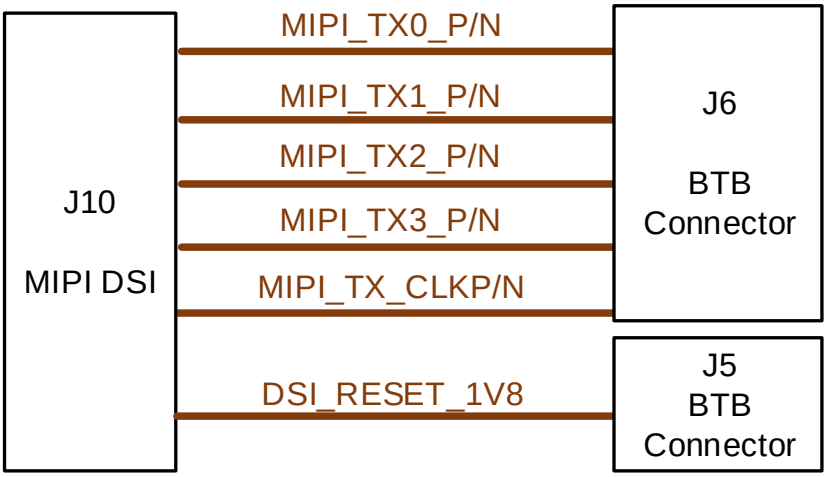


Figure 4-9 Connection Diagram of MIPI DPHY Hard Core Interface

Figure 4-10 Connection Diagram of MIPI DPHY Soft Core Interface

Figure 4-11 Connection Diagram of MIPI DPHY DSI Interface



4.7.2 Pin Distribution

Table 4-7 Pin Distribution of MIPI CPHY Hard Core Interface

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	CPHY0_D2C	J2	MIPI_M1	-	MIPI CPHY data signal
3	CPHY0_D2B	J1	MIPI_M1	-	MIPI CPHY data signal
4	CPHY0_D2A	H1	MIPI_M1	-	MIPI CPHY data signal
5	GND	-	-	-	GND
6	CPHY0_D1C	G2	MIPI_M1	-	MIPI CPHY data signal
7	CPHY0_D1B	G1	MIPI_M1	-	MIPI CPHY data signal
8	CPHY0_D1A	F1	MIPI_M1	-	MIPI CPHY data signal
9	GND	-	-	-	GND
10	CPHY0_D0C	E1	MIPI_M1	-	MIPI CPHY data signal
11	CPHY0_D0B	E2	MIPI_M1	-	MIPI CPHY data signal
12	CPHY0_D0A	D1	MIPI_M1	-	MIPI CPHY data signal
13	GND	-	-	-	GND
14	CAM_RESETN_1V8	J5	10	1.8V	Reset signal
15	CAM_SDA_1V8	H6	10	1.8V	I2C data signal
16	CAM_SCL_1V8	H5	10	1.8V	I2C clock signal
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	VDD3V3	-	-	3.3V	Power
20	VDD3V3	-	-	3.3V	Power

Table 4-8 Pin Distribution of MIPI DPHY Hard Core Interface

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	VDDDPHY	-	-	5V/3.3V	Power
2	VDDDPHY	-	-	5V/3.3V	Power

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
3	GND	-	-	-	GND
4	DPHY0_D3P	C1	MIPI_M0	-	MIPI DPHY data signal
5	DPHY0_D3N	C2	MIPI_M0	-	MIPI DPHY data signal
6	GND	-	-	-	GND
7	DPHY0_D2P	F4	MIPI_M0	-	MIPI DPHY data signal
8	DPHY0_D2N	E3	MIPI_M0	-	MIPI DPHY data signal
9	GND	-	-	-	GND
10	DPHY0_CKP	G3	MIPI_M0	-	MIPI DPHY clock signal
11	DPHY0_CKN	F3	MIPI_M0	-	MIPI DPHY clock signal
12	GND	-	-	-	GND
13	DPHY0_D1P	H4	MIPI_M0	-	MIPI DPHY data signal
14	DPHY0_D1N	H3	MIPI_M0	-	MIPI DPHY data signal
15	GND	-	-	-	GND
16	DPHY0_D0P	J4	MIPI_M0	-	MIPI DPHY data signal
17	DPHY0_D0N	J3	MIPI_M0	-	MIPI DPHY data signal
18	GND	-	-	-	GND
19	F5/IOL41A/LVDS	F5	11	1.8V	GPIO
20	G5/IOL41B/LVDS	G5	11	1.8V	GPIO

Table 4-9 Pin Distribution of MIPI DPHY Soft Core Interface

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	VDD3V3	-	-	3.3V	Power
2	VDD3V3	-	-	3.3V	Power
3	NC	-	-	-	Floating
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	NC	-	-	-	Floating
7	NC	-	-	-	Floating
8	GND	-	-	-	GND
9	NC	-	-	-	Floating
10	NC	-	-	-	Floating
11	GND	-	-	-	GND
12	MIPI_RX_CLKP	F10	1	1.2V	Receive clock signal of MIPI DPHY
13	MIPI_RX_CLKN	E10	1	1.2V	Receive clock signal of MIPI DPHY
14	GND	-	-	-	GND
15	NC	-	-	-	Floating
16	NC	-	-	-	Floating
17	GND	-	-	-	GND
18	MIPI_RX0_P	C14	2	1.2V	Receive data signal of MIPI DPHY
19	MIPI_RX0_N	D13	2	1.2V	Receive data signal of MIPI DPHY
20	GND	-	-	-	GND
21	CSI_SCL_1V8	H5	10	1.8V	I2C clock signal
22	CSI_SDA_1V8	H6	10	1.8V	I2C data signal
23	NC	-	-	-	Floating
24	NC	-	-	-	Floating
25	GND	-	-	-	GND

Table 4-10 Pin Distribution of MIPI DPHY DSI Interface

J10 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LEDK	-	-	-	Backlight cathode
2	LEDA	-	-	-	Backlight anode
3	GND	-	-	-	GND
4	NC	-	-	-	Floating
5	NC	-	-	-	Floating
6	DSI_RESET_1V8	K4	11	1.8V	Reset signal
7	GND	-	-	-	GND
8	VDD1V8	-	-	1.8V	Power
9	VDD2V8	-	-	2.8V	Power
10	MIPI_TX3_P	B13	2	1.2V	Transmit data signal of MIPI DSI
11	GND	-	-	-	GND
12	MIPI_TX3_N	A13	2	1.2V	Transmit data signal of MIPI DSI
13	MIPI_TX2_P	E7	1	1.2V	Transmit data signal of MIPI DSI
14	MIPI_TX2_N	E8	1	1.2V	Transmit data signal of MIPI DSI
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	MIPI_TX_CLKP	E5	1	1.2V	Clock signal of MIPI DSI
18	MIPI_TX_CLKN	E6	1	1.2V	Clock signal of MIPI DSI
19	GND	-	-	-	GND
20	MIPI_TX1_P	F8	1	1.2V	Transmit data signal of MIPI DSI
21	MIPI_TX1_N	E9	1	1.2V	Transmit data signal of MIPI DSI
22	GND	-	-	-	GND
23	MIPI_TX0_P	B14	2	1.2V	Transmit data signal of

J10 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
					MIPI DSI
24	MIPI_TX0_N	A14	2	1.2V	Transmit data signal of MIPI DSI
25	GND	-	-	-	GND

5 Demo

The demo includes basic demos and image demos. The basic demo is used to validate the board's basic functions such as HDMI, DDR3, LVDS, DSI, and DP. The image demo is used to conduct HDMI and LVDS screen display tests for various cameras based on DDR3, MIPI C-PHY hard core, and MIPI D-PHY soft core. For the details of the demo, see *DBUG1282, DK_VIDEO_GW5AT-LV60UG225_V1.0 Development Board Demo User Guide*.

Table 5-1 Basic Demo Introduction

No.	Project Name	Design Description
1	01_G60_LED_1bit_Test	1 bit LED blinking test
2	02_G60_UART_Test_115200	Serial communication loopback test (115200bps)
3	03-1_G60_HDMI_Display_7200P60	1280*720@60 HDMI screen display test
4	03-2_G60_HDMI_Display_1080P60	1920*1080@60 HDMI screen display test
5	04_G60_LVDS_Display_1024x600	1024*600@60 LVDS LCD screen display test
6	05_G60_DSI_Display_1080x1920	1080*1920@60 MIPI DSI LCD screen display test
7	06_G60_DP_Display_1080P60	1920*1080@60 DP screen display test
8	07_G60_DP_Display_1080P60_RX2TX	1920*1080@ 60 DP screen receiving display test
9	08-1_G60_DDR3_HDMI_Display_1080P60	1920*1080@60 DDR3 image cache and HDMI screen display test
10	08-2_G60_DDR3_LVDS_Display_1024600	1024*600@60 DDR3 image cache and LVDS screen display test

No.	Project Name	Design Description
11	08-3_G60_DDR3_DSI_ Display_10801920	1080*1920@60 DDR3 image cache and MIPI DSI LCD screen display test

Table 5-2 Image Demo Introduction

No.	Project Name	Design Description
1	01-1_SC130GS_DDR3_ HDMI_720P60	SC130GS black-and-white exposure 1-lane HDMI screen display project based on DPHY soft core and DDR3
2	01-2_SC130GS_DDR3_ LVDS_1024600	SC130GS black-and-white exposure 1-lane LVDS screen display project based on DPHY soft core and DDR3
3	02-1_SC2210_DDR3_ HDMI_1080P60	SC2210 color exposure 1-lane HDMI screen display project based on DPHY soft core and DDR3
4	02-2_SC2210_DDR3_ LVDS_1024600	SC2210 color exposure 1-lane LVDS screen display project based on DPHY soft core and DDR3
5	03-1_IMX586_DDR3_HDMI _1080P60	IMX586 1920x1080@60 HDMI screen display project based on CPHY hard core
6	03-2_IMX586_DDR3_LVDS _1024600	IMX586 1024x600@60 LVDS screen display project based on CPHY hard core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